

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	2	6151248.pn.	USPAT; US-P GPUB ; EPO; JPO; DERW ENT; IBM _TDB	2003/04/1 5 17:02	
2	BRS	L2	2	6103573.pn.	USPAT; US-P GPUB ; EPO; JPO; DERW ENT; IBM _TDB	2003/04/1 5 17:10	
3	BRS	L3	180849	(remov\$3 or pattern\$3 or etch\$3) near10 (dielectric or insulat\$3)	USPAT; US-P GPUB ; EPO; JPO; DERW ENT; IBM _TDB	2003/04/1 5 17:12	
4	BRS	L4	9383	(remov\$3 or pattern\$3 or etch\$3) near10 (dielectric or insulat\$3) near15 (polysilicon)	USPAT; US-P GPUB ; EPO; JPO; DERW ENT; IBM _TDB	2003/04/1 5 17:13	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
5	BRS	L5	9	(remov\$3 or pattern\$3 or etch\$3) near10 (dielectric or insulat\$3) near15 uniform near surface near10 (polysilicon)	USPA T; US-P GPUB ; EPO; JPO; DERW ENT; IBM — TDB	2003/04/1 5 17:16	
6	BRS	L6	2169	(remov\$3 or pattern\$3 or etch\$3) near10 (dielectric or insulat\$3) near15 surface near10 (polysilicon)	USPA T; US-P GPUB ; EPO; JPO; DERW ENT; IBM — TDB	2003/04/1 5 17:18	

	<b>U</b>	<b>1</b>	<b>Document ID</b>	<b>Title</b>	<b>Current OR</b>	<b>Pages</b>	<b>Issue Date</b>
1	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20030068860 A1	NON-VOLATILE MEMORY CELLS WITH SELECTIVELY FORMED FLOATING GATE	438/257	14	20030410
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20030017677 A1	Storage electrode of a semiconductor memory device and method for fabricating the same	438/396	16	20030123
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6373109 B1	Semiconductor device to more precisely reflect the claimed invention	257/384	8	20020416
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6110771 A	Fabrication method of a semiconductor device using self-aligned silicide CMOS having a dummy gate electrode	438/200	9	20000829
5	<input type="checkbox"/>	<input type="checkbox"/>	JP 11145145 A	MANUFACTURE OF SEMICONDUCTOR DEVICE HAVING WIRING CONSTITUTED OF DOPED POLYSILICON FILM		6	19990528
6	<input type="checkbox"/>	<input type="checkbox"/>	JP 05166919 A	SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF		8	19930702
7	<input type="checkbox"/>	<input type="checkbox"/>	JP 02303051 A	MANUFACTURE OF SEMICONDUCTOR DEVICE		4	19901217
8	<input type="checkbox"/>	<input type="checkbox"/>	KR 9405626 B	Patterning method - comprises forming poly:silicon layer on insulating layer, forming photoresist pattern on poly:silicon layer, etching poly:silicon layer using chlorine source, etc.		NA	19940621
9	<input type="checkbox"/>	<input type="checkbox"/>	JP 02181934 A	MIS semiconductor with LPD and salicide structure - independently controls location of boundary between high and low impurity density source-drain regions and positions of salicide layers		11	19900716

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